Two-Dimensional Optoelectronic Digital Halftoning Processor

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1 Executive Summary:

To meet the challenge of increasingly higher data volume and processing requirements in military and national security applications, multi-channel optoelectronic (OE) and photonic smart image processors based on optical interconnect technology offer a promising solution because of their unique capability of high-bandwidth, parallel data, and image transmission and processing. The OE smart image processor comprises an integrated array of individually controlled transmission channels and receiving channels.

We designed and fabricated the multi-channel OE processor using 8x8 850-nm VCSEL and InGaAs p-i-n photodetector (PD) arrays. We integrated 64-channel OE image processor in a free-space configuration. The PC board mounted VCSEL transmitter and photoreceiver arrays were optically aligned. Optical image processing was carried out utilizing a diffractive optical element (DOE) device for the fan-out/fan-in interconnection processing functionality. The DOE was fabricated on a transparent quartz substrate with 8-level structural features. When a single VCSEL transmitter channel is aligned to a DOE unit, the transmitted beam delivered a 7x7 diffractive pattern at the back focal-plane of the DOE.

These integrated interconnects were investigated in an OE processing architecture as a digital halftoning image processor. In our experiment, an initial gray-scale image is loaded into the computer for processing by the digital halftoning system. The error by individual pixel is computed with a threshold function and transmitted using the analog channels to the VCSEL array. The VCSELs lase according to the input pattern from the controlling computer. The light output from the VCSEL array is incident upon the diffractive optical element which fans the individual channels out in the 7x7 pattern onto the detector array. The intensities from the various DOE outputs combine through the superposition principle and form the diffused error output. This error output is then read into the computer and forms the new image. This process is iterated until the image is deemed of appropriate quality. The parallel nature of this optical system demonstrates the potential of very high-speed and high-throughput parallel information processing. This paper focuses on the differences in VCSEL physical spacing and the resulting DOE optical diffraction spacing as well as the superposition results for various VCSEL optical power output levels.

2 Introduction and Background

Optics has the potential of performing high-speed, high-throughput parallel information processing. Technology improvements are moving many applications from analog signal processing techniques to digital signal processing. Digital signal processing provides higher resolution, improved flexibility and functionality, and increased noise immunity over its analog counterparts and therefore is the preferred method for accurate signal processing. The challenge becomes therefore to convert the very common analog signal to a digital representation. The analog-to-digital (A/D) interface is generally considered to be the most critical part of the overall signal acquisition and processing system. Achieving both high-resolution and high-speed A/D converters is the current barrier to accurately and quickly processing large amounts of data.

Digital image halftoning is an application of A/D conversion techniques to image processing. Halftoning is the process of optimally representing a continuous-tone or multi-level gray-scale image that is printed or displayed using only *binary-valued* pixels. Halftoning also does compression on the image because of the binary vs. n-bit valued pixels. This particular technique has important applications to Army users in such areas as transmission of high-resolution maps and images to battlefield locations using tactical communication links and facsimile. There are many different halftoning algorithms, each with advantages and disadvantages and with different degrees of effectiveness. Error diffusion is one method of achieving digital halftoning in which the error associated with a nonlinear quantization process is diffused within a local region and subsequent filtering methods employed in an effort to improve some performance metric such as signal-to-noise ratio. Classical error diffusion is a one-dimensional, serial technique in that the algorithm raster scans the image from upper-left to lower-right and as a result, introduces visual artifacts directly attributable to the halftoning algorithm itself. A fully parallel implementation of the error diffusion algorithm, however, provides the advantage that all pixel quantization decisions are computed in parallel and therefore the error diffusion process becomes two-dimensional and symmetric. Visual artifacts attributable to the halftoning algorithm are eliminated and overall halftoned image quality is significantly improved. An optoelectronic implementation of the error diffusion algorithm is one approach to this fully parallel implementation. In addition, the inherent parallelism associated an optical implementation reduces the computational requirements while decreasing the total convergence time of the halftoning process. Shoop and Ressler [1] developed a new artificial neural network architecture based on the mathematical foundation of the error diffusion algorithm called the *error diffusion neural network*. Software simulations of the error diffusion neural network produce visually pleasing results that are missing the artifacts present in other halftoning algorithms.

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We have been developing a hardware implementation of the error diffusion network to parallel the software simulation. The complete optical interconnect system consists of the computer, VCSEL array, diffractive optical element, and detector array. The function of the detector array is being temporarily performed by a charge-coupled detector (CCD). The computer will control the VCSEL array and also the detector array. The data from the original image will be

transmitted through the VCSEL array, processed by the DOE, and then the new data received by the detector array. This process is then iterated until the image is deemed of appropriate quality. The DOE fanout intensities have been characterized [2] and closely match theoretical values. The VCSEL arrays have been characterized for uniformity and for throughput performance [3] and will function at throughput rates far beyond the capabilities of the control computer. Operation of the overall halftoning architecture is described in [4].

4 Experimental Setup

We started this study by characterizing the performance of the VCSEL and the DOE arrays. The experimental setup is shown in Figure 1. A CCD is being used temporarily in place of the detector array to determine both the DOE's optical spacing and its fanout intensities. Up to four VCSELs can be driven individually by current sources and final computer control will have each of the 64 VCSELs controlled separately.

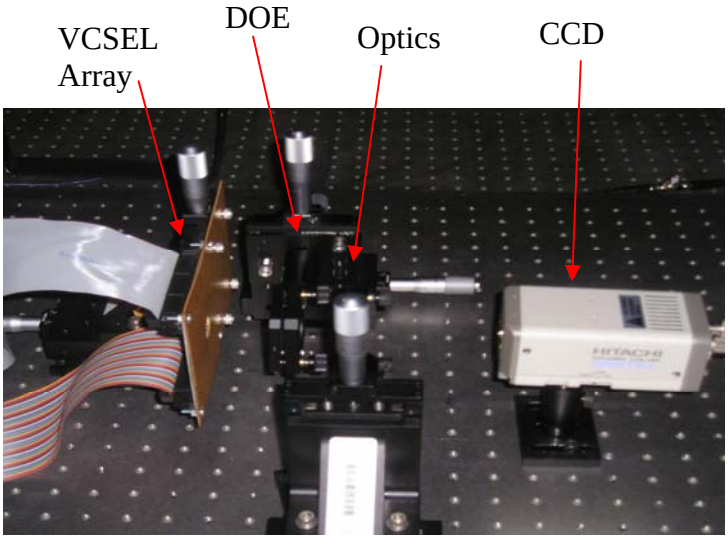


Figure 1. Experimental Setup

4.1 DOE Optical Spacing

The two-dimensional optoelectronic digital halftoning processor architecture relies on a one-to-one spacing relationship for both VCSEL array and the DOE output. We investigated the spacing relationship for the current setup by lighting a complete row and column of VCSELs without the DOE in the setup (Figure 2). The pitch of the VCSEL array is 125 µm in both dimensions as shown in the symmetrical axes.

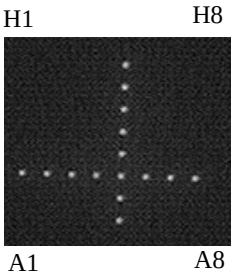
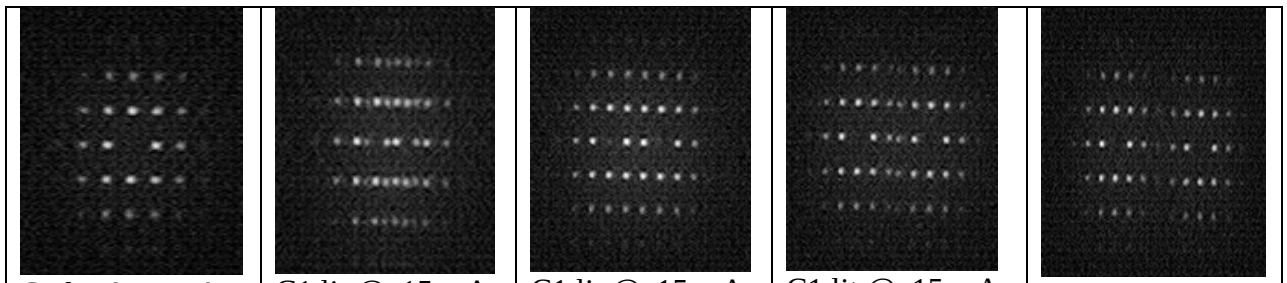


Figure 2. 8x8 VCSEL array with a complete row and column lit

For the horizontal study, the leftmost VCSEL (C1) in the row was lit as a control. The adjacent VCSEL (C2) was then lit and the resulting fanouts of the two VCSELs captured. Figure 3 records the lighting of VCSELs horizontally from left to right. The second image of Figure 3 shows the fanout from the two adjacent VCSELs not being aligned. The output from the left VCSEL (C1) can be distinguished from the right's (C2) output. Again lighting the leftmost VCSEL (C1) in the row, now skipping the second, and lighting the third (C3) produces the third image in Figure 3. This clearly shows the superposition of each output from the right columns of the left VCSEL (C1) and the left columns of the right VCSEL (C3). Careful analysis of the superposition image shows an offset of three DOE spaces between the nulls. The fourth and fifth images in Figure 3 show the results of lighting the next two VCSELs in the row with the leftmost VCSEL (C1). The fourth image shows the same distinct fanout patterns as the second image and the fifth again shows the superposition output. The fifth image only has one column of each VCSEL combining because the patterns are now six spaces apart.



C1 lit 0.15 mA	C1 lit @ .15 mA C2 lit @ .15 mA	C1 lit @ .15 mA C3 lit @ .15 mA	C1 lit @ .15 mA C4 lit @ .15 mA	C1 lit @ .15 mA C5 lit @ .15 mA

Figure 3. DOE results (horizontal)

Figure 4 shows the same procedure applied to the vertical column of the VCSEL array starting at the bottom and moving to the top. The designed DOE pitch is different by a factor of two in the horizontal and vertical directions so we expected equivalent differences in the two cases. Analysis of the images in Figure 4 shows that the fanout pattern moves 0.75 DOE spacing per VCSEL so they superimpose again on every fourth VCSEL.

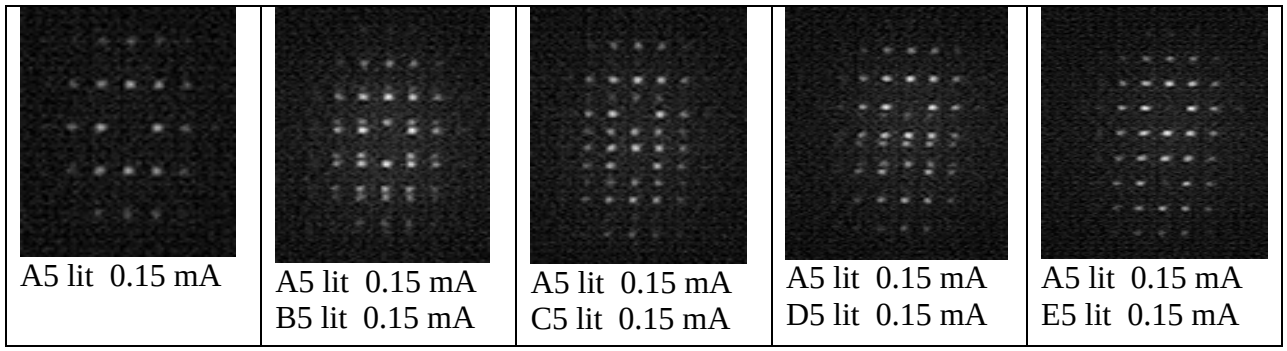


Figure 4. DOE results (vertical)

4.2 DOE Optical Spacing Results

We draw the following conclusions from the outputs in Figures 3 and 4: 1) the horizontal case shows that 1 VCSEL shift gives a 1.5 DOE shift in spacing; 2) the vertical case shows that 1 VCSEL shift gives a 0.75 DOE shift; 3) the horizontal and vertical cases do show the expected 2:1 spacing. Other images captured with similar horizontal and vertical pairs support all of the above conclusions. Figure 5 shows the resulting expected symmetrical "squared" output when lighting the appropriate input VCSELs using the above conclusions.

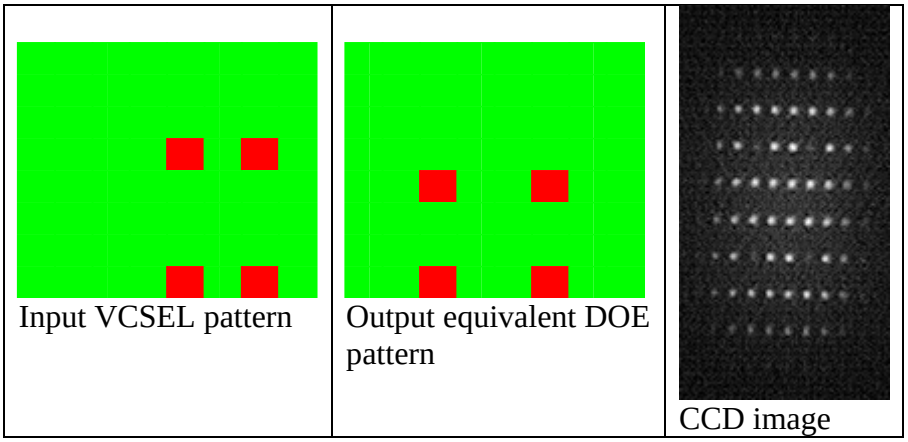


Figure 5. Superposition of four appropriately-spaced VCSELs

The current DOE fanouts are not useful for the full digital halftoning implementation since the optical interconnections are only for every third element both horizontally and vertically. This will be rectified by using different bulk optics for focusing so that adjacent VCSELs do produce fanouts with adjacent superposition. The 2:1 difference between the horizontal and vertical dimensions will be fixed with a cylindrical lens.

5 Optical Intensities

A subjective study of the superposition results from two VCSELs was also performed. The top row of Figure 6 shows the fanout from a single VCSEL that is lit at various input currents. The result from the higher input current shows the outer ring of the 7x7 fanout which are indistinguishable at lower input currents. The bottom row shows a VCSEL pair physically aligned vertically with a separation of four VCSELs as in paragraph 4. The bottom VCSEL is held constant at 0.3 mA input current while the upper VCSEL is driven from 0.3 mA to 0.8 mA. The resulting images subjectively show the expected changes in output. Of special note is the bottom right image showing the null of the bottom VCSEL being lit by the last row of the fanout from the top VCSEL.

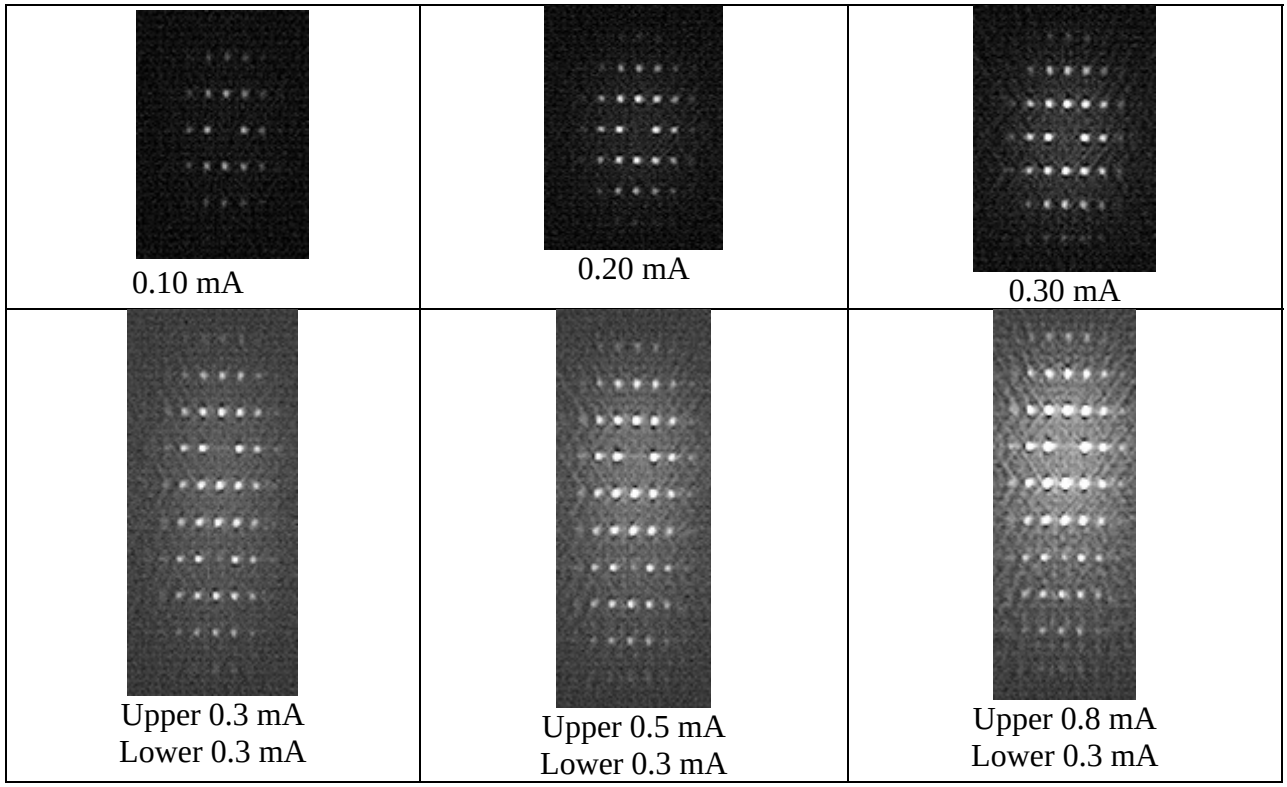


Figure 6. DOE Fanout Superposition from various intensities

8 Future Work

The current experimental setup does not have the correct DOE fanout alignment. This will be corrected by using different bulk optics and a cylindrical lens. The output intensities from a superposition image need to be objectively analyzed using appropriate measurement equipment. The CCD used as an interim step in the opto-electronic digital halftoning system needs to be replaced with the detector array to implement the rest of the processor.

8 Conclusions

The two-dimensional optoelectronic digital halftoning processor promises to deliver fast and parallel data rates with very low power consumption. The studies in this paper show the possibility of implementing this processor.

References

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[4] J. J. Liu, B. R. Gollsneider, B. Shoop, W. Chang, G. Simonis, "Two-Dimensional Optoelectronic Digital Halftoning Processor", The 12th Annual Army Research Laboratory/United States Military Academy Technical Symposium, (West Point, New York), November 2004.